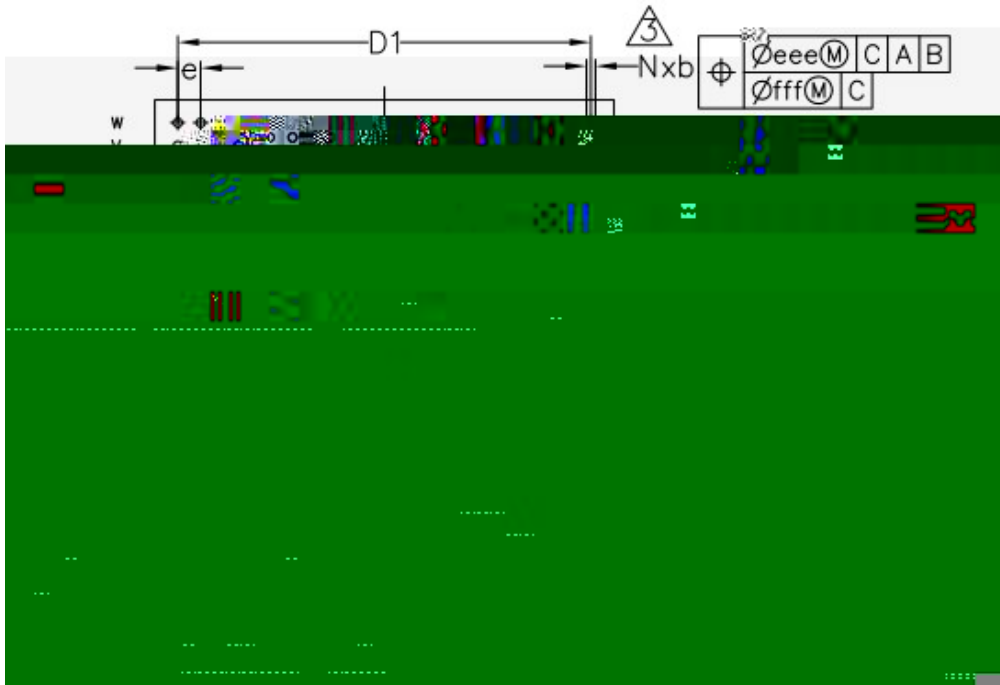
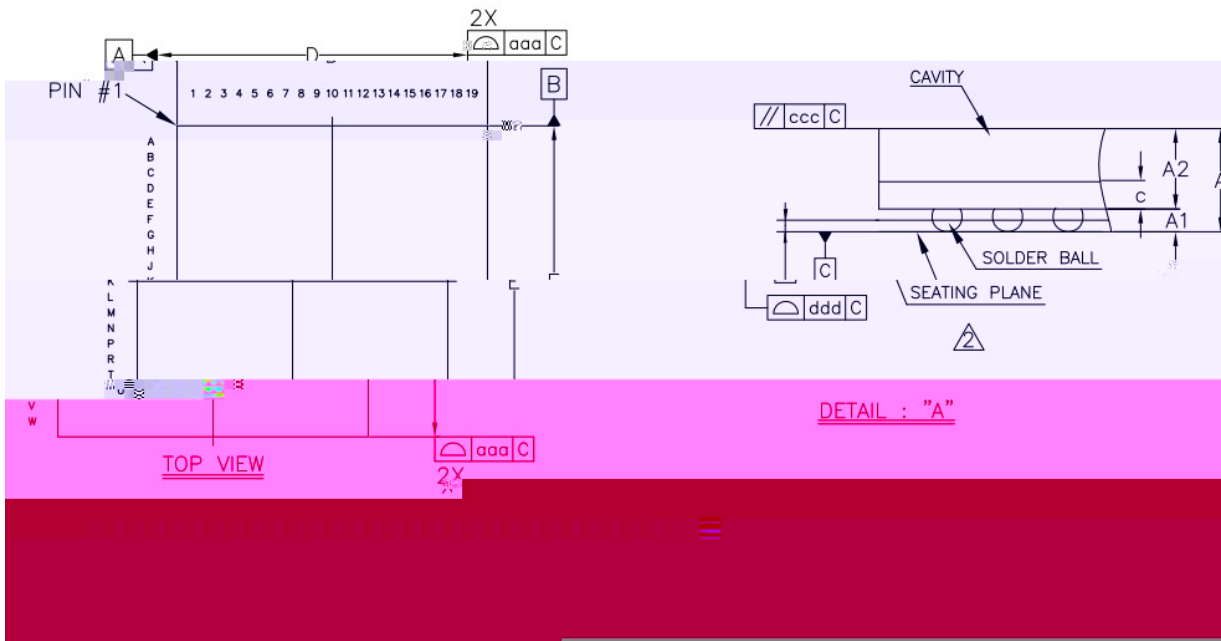




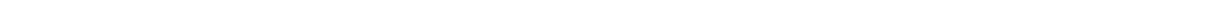
Table of Contents





	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19				
A	GND_PEP HY_GD	PE_TX_N 3	GND_PEP HY_GD	PE_RX_N 3	PE_RX_N 2	GND_PEP HY_GD	PE_TX_N 2	PE_TX_N 1	GND_PEP HY_GD	PE_RX_N 1	PE_RX_N 0	GND_PEP HY_GD	PE_TX_N 0	UART_SRX IV_0	SPI_CLK_D IV_0	NO_GPIO 1	N2_GPIO 1	N3_GPIO 1	GND				
B	GND_PEP HY_GD	PE_TX_P 3	GND_PEP HY_GD	PE_RX_P 3	PE_RX_P 2	GND_PEP HY_GD	PE_TX_P 2	PE_TX_P 1	GND_PEP HY_GD	PE_RX_P 1	PE_RX_P 0	GND_PEP HY_GD	PE_TX_P 0	SPI_CLK_D IV_2	N1_GPIO 1	PE_RST_S EQ	SPI_CLK	URST_N	JTDI				
C	MNG_BSY	MII_MD	VCC33_N3 EFUSE	VCC33_N1 EFUSE	VCC33_NO EFUSE	GND_TS GND33A	VCC33A_1 DC	PE_REF_C LK_P	GND_PEP HY_GD	PE_PHY_R ESREF	GND_PEP HY_GD	PRB_HIT	PRB_CLKO UT	MNG_GPIO O_1	SPI_SI	JTMS	NO_DIS_N	N2_DIS_N	JTAG_SEL 1				
D	PRB_EN	PCIE_BSY	MII_MDC	VCC33_EF USE	VCC33_N2 EFUSE	GND_PEP HY_GD	VCC11A_P E_VP	PE_REF_C LK_N	VCC11A_P E_VP	GND_PEP HY_GD	UART_STX	NO_GPIO 0	N2_GPIO 0	MNG_GPIO O_0	PE_AUX_P WR_DET	SPI_CS_N	SPI_SO	JTDO	N2_RGMII TX_0				
E	CLK_TST_S EL_1	CLK_TST_S EL_3	USE_EXT PHY	CLK_TST_S EL_0	CLK_TST_S EL_2	VCC11A_P E_VPTX3	VCC11A_P E_VPTX2	VCC33A_P E_VPH	VCC11A_P E_VPTX1	VCC11A_P E_VPTX0	VCCCK_VM AIN	SPI_CLK_D IV_1	N1_GPIO 0	N3_GPIO 0	PE_WAKE N	JTAG_SEL 0	N1_DIS_N	N2_RGMII TX_1	N2_RGMII RX_1				
F	TEST_SEL DE_0	TEST_SEL DE_2	MNG_DET DE_1	TEST_SEL DE_3	TEST_SEL										JTCK	N3_D_S_N	N3_RGMII TX_1	N2_RGMII TX_2	N2_RGMII RX_2				
G	SEC_DISA BLE	SCAN_EN ABLE	PERST_N	FLASH_SE CTOR	POR_BYP ASS	VCC310									VCC6	VCC310	VCC310	N3_RGMII TX_2	N3_RGMII TX_0	N3_RGMII TX_3	N2_RGMII TX_3	N2_RGMII RX_3	
H	NO_LED_0	NO_LED_1	NO_LED_2	NO_LED_3	NO_LED_4	VCC310									VCC6	VCC310	VCC310	N3_BGMII RX_0	N3_BGMII TX_0	N3_BGMII TX_1	N2_BGMII TX_2	N2_BGMII RX_2	
I	NO_LED_0	NO_LED_1	MNG_C SMBUS	MNG_C CLK	RMI_CSR _DV	VCC310									VCC6	VCC310	VCC310	N3_BGMII RX_3	N3_BGMII TX_CTL	N3_BGMII MDIO	N2_BGMII RX_CTL	N2_BGMII MDC	K
J	NO_LED_0	NO_LED_1	RMI_TXD	RMI_TX	NO_TS158	VCC310									VCC6	VCC310	VCC310	N3_BGMII RX_3	N3_BGMII TX_CTL	N3_BGMII MDIO	N2_BGMII RX_CTL	N2_BGMII MDC	K

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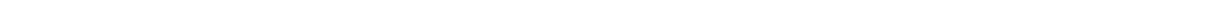
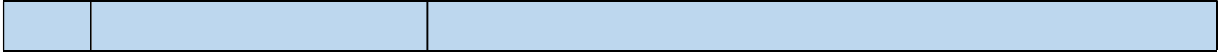




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	-65		140	° C
Tj(FN)	-55		125	° C
VCK VCI1A	-01	11	115	V
VCI1A_FE; VCI1A_AIO VCI1A_CEN; VCI1A_HL	-01	11	115	V
VCI1Q; VCI3A VCI3	-04	33	37	V
VCI1O; VCI25V	-04	33	37	V

32

	-40		85	° C
VCK VCI1A	105	11	115	V
VCI1A_FE; VCI1A_AIO VCI1A_CEN; VCI1A_HL	105	11	115	V
VCI1Q; VCI3A VCI3	315	33	345	V
VCI1O; VCI25V	315	33	345	V

33

IOreference vdtage	Vref		30	33	36	V
Input low vdtage	Vl				08	V
Input high vdtage	Vh		20			V
Input low current	Iil	Vin=0V	-20		0	μA
Input high current	Iih	Vin=Vref- Vref, max	0		200	μA
Output low vdtage	Vl	Id=-4nA Vref=rin	0		400	nW
Output high vdtage	Vh	ICh=- 4nA Vref=rin	24		Vref	V

34

3.1.1 NCSI AC Specification

Tck	NSI_REF_CLK Frequency		50		NE
Rdc	NSI_REF_CLK duty cycle	35		65	%
Racc	NSI_REF_CLK accuracy			100	ppm
Tco	Clock to out (10 pF \times load \leq 50 pF) NSI_EQ1 Q , NSI_SRIV Data valid from NSI_REF_CLK rising edge	2.5		12.5	ns
Tsu	NSI_EQ1 Q , NSI_TXEN Data Setup to NSI_CLKIN rising edge	3			ns
Thdd	NSI_EQ1 Q , NSI_TXEN Data hold from NSI_REF_CLK rising edge	1			ns
Tr	NSI_EQ1 Q , NSI_SRIV Output Time rise	0.5		6	ns
Tf	NSI_EQ1 Q , NSI_SRIV Output Time fall	0.5		6	ns
Tdr/Tdf	NSI_REF_CLK Rise/Fall Time	0.5		3.5	ns

34

Frequency	-	-	25	-	NE
Frequency Stability	Ta=0 70	-30		+30	ppm
Frequency Tolerance	Ta=25	-50		+50	ppm
Duty Cycle		40		60	%
Broadband Peak to peak Jitter				200	ps
Vpeak to peak		3.135	3.3	3.465	V



Rise time 10%90%				10	ns
Fall time 10%90%				10	ns
Operation temperature Range		0		70	

35

CHY IP 1 IV 33V 5ms 33V rise time 1ns
33V 1 IV

Rt1	33V rise time	1	-	
Rt2	33V ready to 1 IV ready time	-5	-	

vrbord	V5Q0V
microchip	SS125AF080B
	CD5Q0

1	VN8002		0 - 70 , 4m ²	2
2	VN8002S		0 - 70 , 4m ² , SM/SN/SM	2
3	VN8004		0 - 70 , 4m ⁴	4
4	VN8004S		0 - 70 , 4m ⁴ , SM/SN/SM	4
5	VN8002L2		-40 - 85 , 4m ²	2
6	VN8002LS		-40 - 85 , 4m ² , SM/SN/SM	2
7	VN8004L4		-40 - 85 , 4m ⁴	4
8	VN8004LS		-40 - 85 , 4m ⁴ , SM/SN/SM	4

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